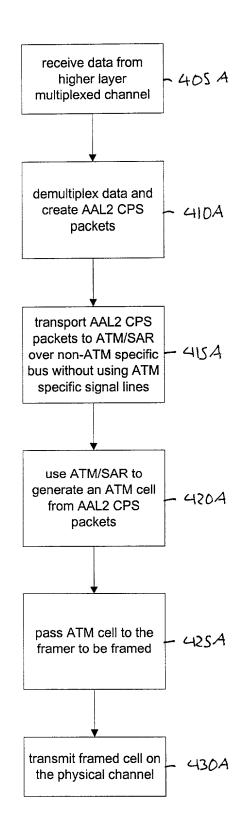
Higher Layers
ATM Adaptation Layers (AALs)
ATM Layer
Physical Layer

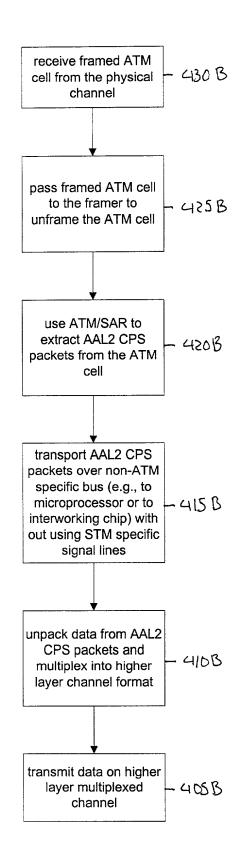
<u>4</u> [7

F18.2A	CID = channel identifier LI = length indicator UUI = user to user indication HEC = header error control	CID 8 bits	CPS Packet Header (CPS-PH)  D LI UUI HEC 6 bits 5 bits 5 bits  AAL2 CPS P	UUI 5 bits AA	S-PH) — C C CPS Packet	CPS-Packet Payload (CPS-PP) CPS-INFO 1 to 64 octets  Packet
5.5.2B	CPS-PDU Header 1 octet	47 octets	CPS-PD	U Payload (AAL2 AAL2 CPS-PDU	id (AAL2 PS-PDU	CPS-PDU Payload (AAL2 CPS Packet(s))  AAL2 CPS-PDU
A1 5 octets	ATM Cell Header tets 48 octets		ATM Cell Payload (CPS-PDU)	l Payload ((	CPS-PDI	(n

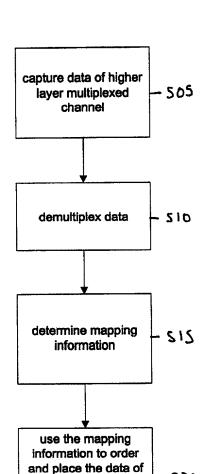
Fis. 2C



413.4A



Fis.4B

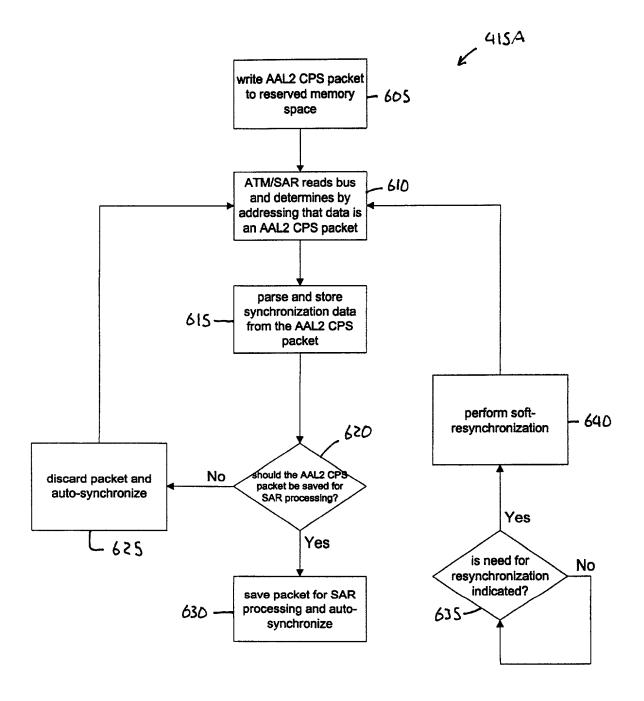


410A

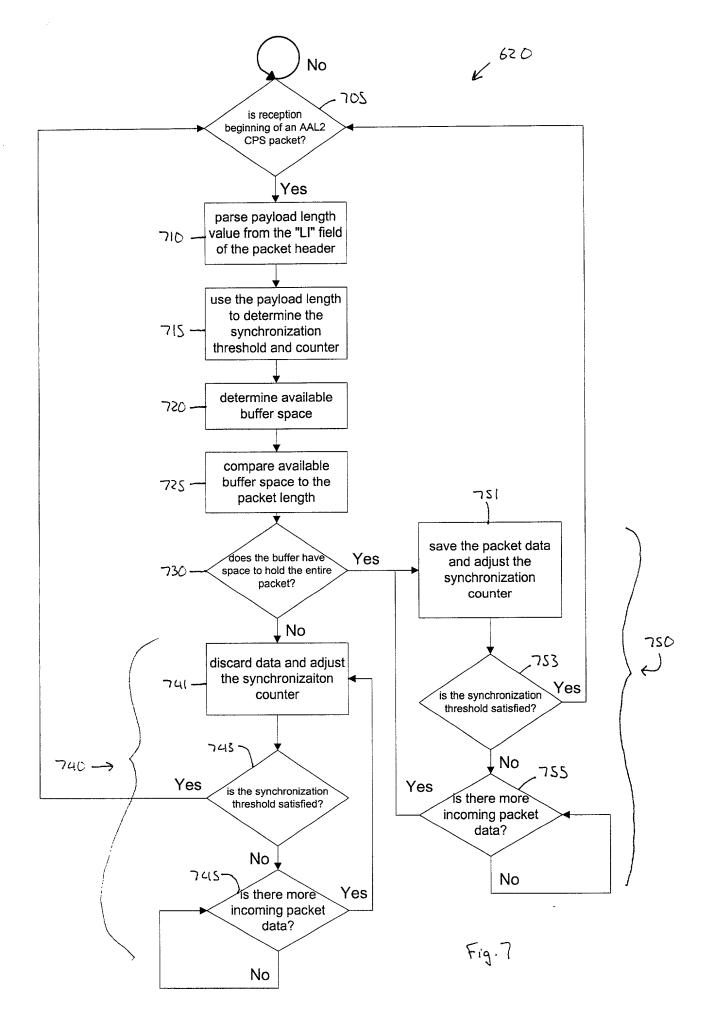
Fis. 5

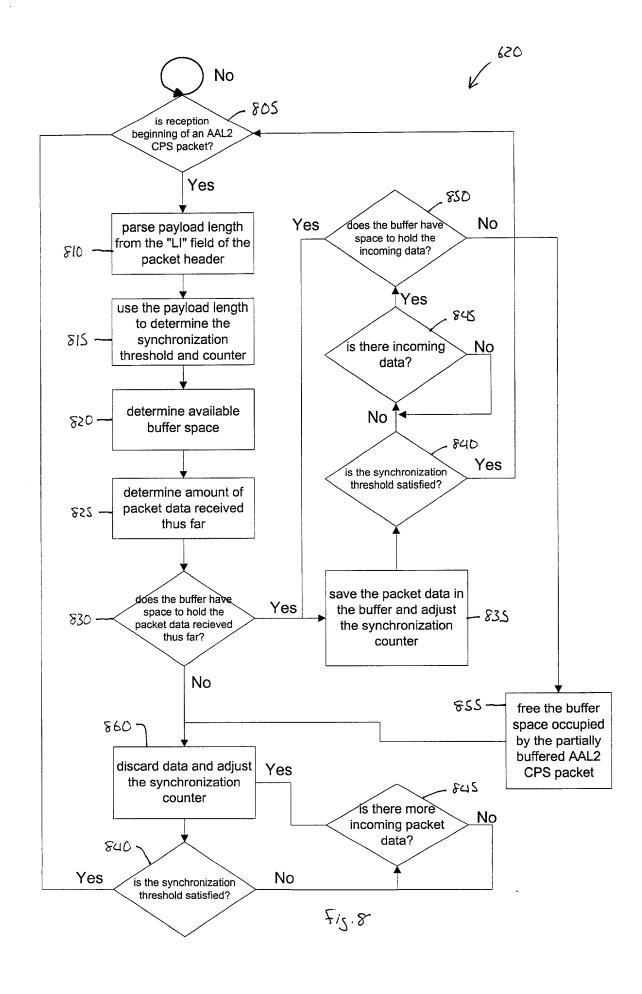
the higher layer multiplexed channel in AAL2 CPS packets in virtual channels 250

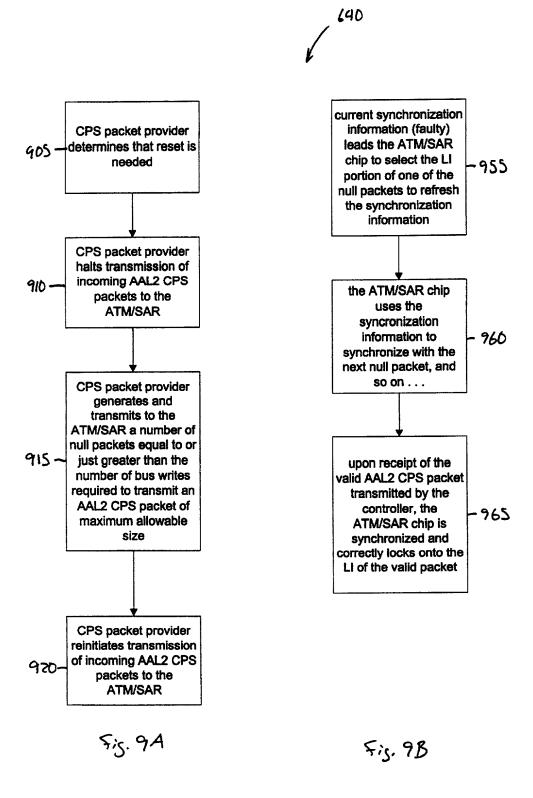
-



Fis. 6

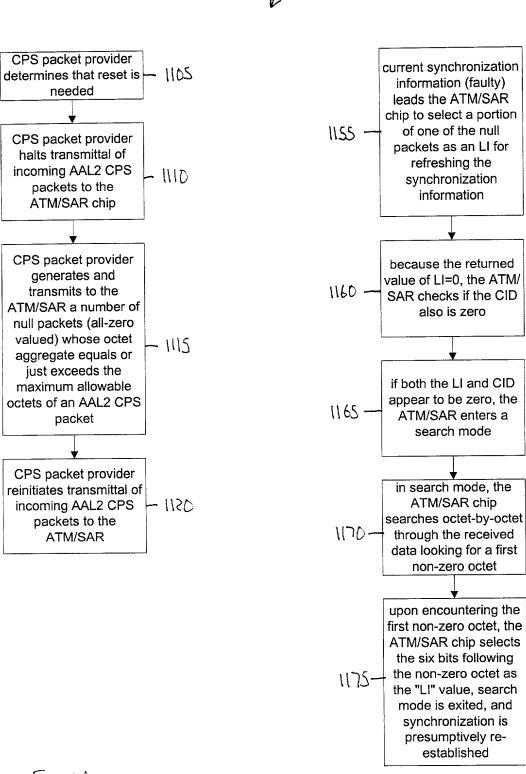






Ξ

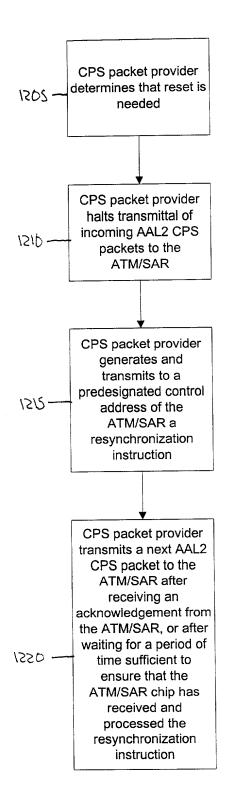
-Null Packet-



640

Fig. 11A

Fig. 11B



upon receiving a resynchronization instruction, the - 1522 ATM/SAR chip halts processing of the current AAL2 CPS packet the ATM/SAR chip may or may not provide an - 1260 acknowledgement to the controller the ATM/SAR chip awaits receipt of the 1565 next AAL2 CPS packet upon which it will resynchronize

Fis. RA

Fig. 12B